

UTILITY
PATENT APPLICATION
TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.

35.C12395 CIP

First Named Inventor or Application Identifier

YOSHIHIKO FUKUMOTO

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification Total Pages 30

3. ☒ Drawing(s) (35 USC 113) Total Sheets 15

4. ☒ Oath or Declaration Total Pages 2

- a. ☐ Newly executed (original or copy)
b. ☒ Unexecuted for information purposes
c. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]

i. ☐ DELETION OF INVENTOR(S)
Signed Statement attached deleting inventor(s)
named in the prior application, see 37 CFR
1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference (useable if Box 4c is checked)
The entire disclosure of the prior application, from which a copy of the
oath or declaration is supplied under Box 4c, is considered as being
part of the disclosure of the accompanying application and is hereby
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EL293309455US

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6. ☐ Microfiche Computer Program (Appendix)

7. Nucleotide and/or Amino Acid Sequence Submission
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- a. ☐ Computer Readable Copy
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ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations
12. ☒ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
14. ☐ Small Entity Statement filed in prior application ☐ Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
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16. ☒ Other: Petition for Extension of Time for three (3) months
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10/28/99
JCS45 U.S. PTO
09/429530
The PTO did not receive the following listed item(s): Petition for Extension

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☒ Continuation-in-part (CIP) of prior application No. 08/979,957 and 08/714,437

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CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
TOTAL CLAIMS (37 CFR 1.16(c))		34-20 =	14	X \$ 18.00 =	\$ 252.00
INDEPENDENT CLAIMS (37 cfr 1.16(b))		3-3 =	0	X \$ 78.00 =	\$.00
MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))				\$260.00 =	\$
				BASIC FEE (37 CFR 1.16(a))	\$ 760.00
				Total of above Calculations =	\$ 1,012.00
Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).					
				TOTAL =	\$ 1,012.00

19. Small entity status

- a. ☐ A Small entity statement is enclosed
- b. ☐ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
- c. ☐ Is no longer claimed.

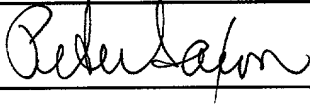
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22. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 06-1205:

- a. ☒ Fees required under 37 CFR 1.16.
- b. ☒ Fees required under 37 CFR 1.17.
- c. ☐ Fees required under 37 CFR 1.18.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

NAME	PETER SAXON
SIGNATURE	
DATE	October 28, 1999

35.C12395 CIP

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
YOSHIHIKO FUKUMOTO)
Application No.: C-I-P of)
08/979,957 and :
08/714,437)
Filed: Herewith)
For: METHOD FOR)
FABRICATING :
SEMICONDUCTOR DEVICE) October 28, 1999

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Contemporaneous with the filing of the subject
application, kindly amend the application as follows:

IN THE SPECIFICATION:

Page 1, line 2, insert

"Express Mail" mailing label number EL 29330945545
Date of Deposit OCTOBER 28, 1999
I hereby certify that this paper or fee is being deposited
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GREGORY FRIPP
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Gregory Fripp
(Signature of person mailing paper or fee)

--This application is a continuation-in-part of Application No. 08/979,957, filed November 26, 1997, now abandoned and Application No. 08/714,437, filed September 16, 1996, the disclosures of which are incorporated by reference.--

Page 1, line 14, "in" should read --in a--;
line 16, "tendency" should read --
development--.

Page 2, line 3, "forming" should read --forming an
isolated--;

line 4, delete "isolation--;
line 8, delete "deposit--;
line 10, delete "feature of--;
line 13, delete "having been--.

Page 4, line 24, "as called the" should read --in
the form of a--.

Page 5, line 15, "is also" should read --has also
been--;

line 16, delete "it";

line 17, "is the present status that"

should read --as presently employed--.

IN THE CLAIMS:

Please cancel claims 1-10 without prejudice or disclaimer.

Kindly add claims 11-44 as follows:

--11. A fabrication method of a semiconductor device comprising:

(a) forming, on a substrate, an insulating film at which at least one of a wiring pattern or a contact pattern is formed;

(b) forming a metal in the at least one of the wiring pattern or the contact pattern;

(c) polishing a surface of the metal; and

(d) washing the polished surface of the metal by (i) conducting an ultrasonic wave washing of said polished surface employing a washing liquid; and (ii) conducting a physical washing of said polished surface after the ultrasonic wave washing.

12. A fabrication method of a semiconductor device according to claim 11, wherein said polishing step (c) is conducted employing chemical mechanical polishing.

13. A fabrication method of a semiconductor device according to claim 11, wherein said ultrasonic wave washing is carried out at a frequency band of not less than 800 kHz.

14. A fabrication method of a semiconductor device according to claim 13, wherein said frequency band is a range of 1 MHz to 3 MHz.

15. A fabrication method of a semiconductor device according to claim 11, wherein said ultrasonic wave washing is carried out while said washing liquid is discharged from a nozzle.

16. A fabrication method of a semiconductor device according to claim 11, wherein said ultrasonic washing is carried out while the substrate with said polished surface thereon is rotated at 1000-2500 rpm.

17. A fabrication method of a semiconductor device according to claim 11, wherein said physical washing is conducted by brush scrubbing or high-pressure jet washing.

18. A fabrication method of a semiconductor device according to claim 11, wherein said physical washing is carried out using a sponge.

19. A fabrication method of a semiconductor device according to claim 18, wherein said sponge comprises polyvinyl alcohol.

20. A fabrication method of a semiconductor device according to claim 11, wherein ultrasonic washing is repeated after said physical washing.

21. A fabrication method according to claim 11, wherein the at least one of said wiring pattern or said contact pattern is formed by forming the insulating film and etching the insulating film.

22. A fabrication method according to claim 11, wherein said insulating film comprises a plurality of laminated insulating layers.

23. A fabrication method according to claim 22, wherein said insulating film includes a first insulating layer having a polished surface and a second insulating layer formed thereon.

24. A fabrication method according to claim 23, wherein said insulating film further includes a third insulating layer formed of a material different from that of said second insulating layer.

25. A fabrication method according to claim 11, wherein said metal is Al, Cu, Au, Cr, Mo, Pt, Ti or an alloy thereof.

26. A fabrication method according to claim 25, wherein said alloy is AlSi, AlCu or AlSiCu.

27. A fabrication method according to claim 11, including forming a barrier metal prior to forming the metal.

28. A fabrication method according to claim 11, wherein said metal is additionally formed on a top surface of said insulating film.

29. A fabrication method according to claim 11, wherein the polishing of a surface of said metal is conducted until the metal surface is at the same level as a top surface of said insulating film.

30. A fabrication method according to claim 11, wherein said polishing step is performed by a polishing with a slurry containing an abrasive.

31. A fabrication method according to claim 11, wherein said washing liquid is pure water.

32. A fabrication method according to claim 11, wherein the ultrasonic wave washing is conducted to reduce an amount of abrasive particles adhered to the polished surface and, thereafter, the amount of abrasive particles is further reduced by the physical washing.

33. A fabrication method of a semiconductor device comprising:

- (a) forming, on a substrate, an insulating film at which a concave section is formed;
- (b) forming a metal in the concave section;
- (c) polishing a surface of the metal; and
- (d) after subjecting the polished surface to an ultrasonic wave washing, further subjecting the polished surface to a physical washing.

34. A method of cleaning a semiconductor device having a polished metal surface, comprising:

- (a) subjecting the polished metal surface to an ultrasonic wave washing; and thereafter
- (b) subjecting the metal surface to a physical washing.

35. A method according to claim 34, wherein said ultrasonic washing is carried out in a frequency band of not less than 800 kHz.

36. A method according to claim 35, wherein said frequency band is a range of 1 MHz to 3 MHz.

37. A method according to claim 34, wherein said ultrasonic wave washing is carried out while said washing liquid is discharged from a nozzle.

38. A method according to claim 34, wherein said ultrasonic wave washing is carried out while the substrate with said polished surface thereon is rotated at 1000-2500 rpm.

39. A method according to claim 34, wherein said physical washing is conducted by brush scrubbing or high-pressure jet washing.

40. A method according to claim 34, wherein said physical washing is carried out using a sponge.

41. A method according to claim 40, wherein said sponge comprises polyvinyl alcohol.

42. A method according to claim 34, wherein said ultrasonic washing is repeated after said physical washing.

43. A method according to claim 34, wherein said washing water is a pure water.

44. A method according to claim 34, wherein the ultrasonic wave washing is conducted to reduce an amount of abrasive particles adhered to said polished surface and, thereafter, the amount of the abrasive particles is further reduced by said physical washing.--

REMARKS

This is a continuation-in-part of Application Nos. 08/979,957 and 08/714,437.

In parent Application No. 08/979,957 the claims were rejected as obvious over Omika '496 in view of Ueda '646. A separately filed information disclosure statement will make of record information from the parent application and other information. The Examiner has cited Omika '496 at column 4, line 5, as teaching "a process for polishing a film." However, it is submitted the cited passage merely

discloses polishing of a substrate surface before a film is formed. Accordingly, Omika fails to disclose polishing a metal deposited in a pattern of an insulating film. It is also submitted that the above art fails to teach the steps of washing the polished surface of the metal formed in the pattern by ultrasonic washing and thereafter subjecting the surface to a physical washing.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,



Attorney for Applicants

Registration No. 24947

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New York, New York 10112-3801
Facsimile: (212) 218-2200

[illegible][illegible][illegible]

	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2
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[illegible][illegible]

an insulation film of BPSG, SiO_2 , or the like deposited on the steps of devices such as transistors, wires, and so on; the recess CMP is a technique for forming buried element isolation, a trench capacitor, a contact plug, or damascene wiring by burying an insulation film of SiO_2 or the like or a metal film of poly-Si, Al, Cu, W, or the like in a hole or a trench formed on a device and removing the deposit film deposited on portions except for the hole or trench portion by polishing. Either of the techniques has the feature of capability of realizing global flatness, when compared with the SOG planarization technology and etch back planarization technology having been used heretofore.

Under such circumstances, it is considered that the layer-insulation-film-flattening CMP technology and the conventional wiring forming technology are adaptable to fabrication of LSI of $0.25\text{-}\mu\text{m}$ and larger rules, but for $0.18\text{-}\mu\text{m}$ and smaller rules, the buried wiring structure by dual damascene using the metal CMP technology will become essential for formation of multilayered wiring, because of factors such as the limit of etching technology of wiring material and guarantee of electromigration resistance.

A buried wiring forming method by dual damascene using the metal CMP will be described below referring to Fig. 26 to Fig. 32.

In Fig. 26, reference numeral 1 designates a

p-type semiconductor substrate, 2 n-type wells, 3 high-concentration p⁺-type source electrodes, 4 high-concentration p⁺-type drain electrodes, and 5 gate electrodes, and low-concentration p⁻-type electric field relaxing regions 3', 4' for increasing the withstand voltage of transistor are provided around the source electrodes 3 and drain electrodes 4. Numeral 6 denotes selective oxide regions for element isolation.

Then, as shown in Fig. 27, NSG (non-doped glass) 7 is deposited by CVD or TEOS and thereafter this NSG 7 is polished and flattened by CMP. The CMP employed herein is polishing using an abrasive cloth, which is a lamination of a foam cloth such as IC-1000 generally used for CMP of layer insulation film and a cloth of nonwoven fabric type, and a silica-based slurry such as SC-1 using fumed silica. Then p-SiN (silicon nitride film formed by the plasma enhanced CVD process) 8 is deposited and thereafter p-SiO (silicon oxide film formed by the plasma enhanced CVD process) 9 is deposited.

Next, as shown in Fig. 28, wiring pattern 10 is formed in the p-SiO 9 by resist patterning and dry etching. On the occasion of the dry etching the p-SiN 8 is used as an etching stopper, whereby the wiring pattern 10 can be formed on a stable basis. Then contact pattern 11 is formed by resist patterning and dry etching.

Subsequently, as shown in Fig. 29, wiring material 12 is deposited. A method for depositing the wiring material 12 herein may be selected from a variety of methods, among which a sputter reflow method of Al- or Cu-based metal material is effective in terms of production cost, reliability, and enhancement of characteristics of device. An effective way to enhance the reliability and reflow characteristics is to form a layer of barrier metal such as Ti/TiN as a ground layer, prior to the above deposition by sputter reflow.

Next, as shown in Fig. 30, the CMP for metal is carried out to polish and flatten the wiring material 12, thereby forming buried wiring 13. The above described the method for forming the buried wiring by dual damascene. By the like method wiring 13' of the second layer and wiring 13" of the third layer can be formed as shown in Fig. 31 and Fig. 32, thereby obtaining the further multilayered structure of wiring.

As described above, the polishing by CMP is effective as means for planarization, but also has some points to be improved. One of them is the problem of washing after the CMP. Since the CMP step itself is a polishing step for machining the wafer surface with the abrasive as called the slurry, abrasive particles of the slurry and chips and products produced in the polishing step are adhering to the wafer surface after the CMP. These must be removed by washing. Since the

wiring material is the Al- or Cu-based metal material,
chemical washing with an acid or an alkali would pose
the problem of corrosion thereof and is thus hardly
applicable. Sufficient cleanliness is not achieved by
5 only washing with pure water. As for scrubbing
washing, which is physical washing using pure water,
and a PVA sponge or a mohair brush, because the wiring
material is the soft metal material, dust particles
adhering to the wafer surface would be the cause of
10 production of fine flaws called scratches on the
surface of wiring material, which would pose the
problem in reliability, such as electromigration.

In addition to the above methods, a washing
method, for example, using field-ionized water with a
15 low metal etching property is also proposed (H. Aoki,
et al., 1994 VLSI Technical Dig., p 79 (1994)), but it
is the present status that the abrasive particles
adhering to the wafer surface cannot be sufficiently
removed by this method.

20

SUMMARY OF THE INVENTION

An object of the present invention is to provide a
fabrication method of semiconductor device comprising,
after formation of an electroconductive material film,
25 a step capable of stably washing a surface of the
electroconductive material film at high cleanliness
without corrosion thereof and without production of

scratch.

Another object of the present invention is to provide a fabrication method of semiconductor device comprising a step of forming an electroconductive
5 material film on a substrate, a step of polishing the electroconductive material film, and a step of washing a polished surface of said electroconductive material film, wherein said washing step is a step of carrying out ultrasonic washing with a washing solution to which
10 an ultrasonic wave is applied, prior to physical washing.

According to the present invention, the polished surface of the electroconductive material film is washed using the washing solution to which the
15 ultrasonic wave is applied, prior to the physical washing, whereby chips made by polishing and abrasive particles of slurry can be effectively removed. By this method, the electroconductive material film for forming the wiring, electrodes, etc, can be washed
20 without production of scratch, or with very little production thereof, and with high cleanliness. The fabrication method of semiconductor device according to the present invention as described can provide a semiconductor device having the electroconductive
25 material member with the extremely flat surface, without a scratch, and with excellent reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an explanatory drawing of the first embodiment of the fabrication method of semiconductor device according to the present invention;

5 Fig. 2 is an explanatory drawing of the first embodiment of the fabrication method of semiconductor device according to the present invention;

10 Fig. 3 is an explanatory drawing of the first embodiment of the fabrication method of semiconductor device according to the present invention;

Fig. 4 is an explanatory drawing of the first embodiment of the fabrication method of semiconductor device according to the present invention;

15 Fig. 5 is an explanatory drawing of the first embodiment of the fabrication method of semiconductor device according to the present invention;

Fig. 6 is an explanatory drawing of the first embodiment of the fabrication method of semiconductor device according to the present invention;

20 Fig. 7 is an explanatory drawing of the first embodiment of the fabrication method of semiconductor device according to the present invention;

Fig. 8 is an SEM photograph of Al surface after metal CMP;

25 Fig. 9 is an enlarged photograph of Fig. 8;

Fig. 10 is an optical microscope photograph of a scratch on Al surface;

Fig. 22 is an explanatory drawing of the
5 fabrication method of reflection type liquid-crystal
display device according to the present invention;

Fig. 24 is an explanatory drawing of the
fabrication method of reflection type liquid-crystal
display device according to the present invention;

Fig. 26 is an explanatory drawing of the fabrication method of semiconductor device according to the conventional example;

Fig. 28 is an explanatory drawing of the fabrication method of semiconductor device according to the conventional example;

Fig. 29 is an explanatory drawing of the fabrication method of semiconductor device according to the conventional example;

Fig. 30 is an explanatory drawing of the fabrication method of semiconductor device according to the conventional example;

Fig. 31 is an explanatory drawing of the fabrication method of semiconductor device according to the conventional example;

Fig. 32 is an explanatory drawing of the fabrication method of semiconductor device according to the conventional example; and

Fig. 33 is an explanatory drawing to show the configuration of a washing apparatus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A fabrication method of semiconductor device according to the present invention is a fabrication method of semiconductor device comprising a step of forming an electroconductive material film on a substrate, a step of polishing the electroconductive material film, and a step of washing a polished surface of said electroconductive material film, wherein said washing step is a step of carrying out ultrasonic washing with a washing solution to which an ultrasonic wave is applied, prior to physical washing.

In the present invention the "electroconductive material" means any material generally used as a wiring material or as an electrode material in the fields of semiconductor industries.

Specific examples of the electroconductive material are Al, Au, Cr, Mo, Pt, Ti, Pt, and polysilicon, used as metal for wiring, metal for barrier, metal for close fit, metal for contact, metal for
5 buffer, or the like, or alloys thereof, ITO (Indium Tin Oxide) used as a transparent electrode, and so on.

A method for film formation of these electroconductive materials is selected from sputtering, vacuum vapor deposition, CVD (Chemical
10 Vapor Deposition), and so on, and the method is not limited to these.

The polishing method of the electroconductive material film can be suitably selected depending upon characteristics and applications of the film, but a
15 preferably applicable method is the chemical mechanical polishing (CMP).

An example of the chemical mechanical polishing (CMP) applicable herein is a method for removing reaction products produced by chemical reaction between
20 the chemical component contained in the abrasive and the polished sample surface, by mechanical polishing with the abrasive and the abrasive cloth. The process of CMP involves a step of mounting the sample to be polished on a rotatable polishing head and a step of
25 thereafter carrying out polishing as pressing the surface of the polished sample against a rotating platen (abrasive plate). A pad (abrasive cloth) is

bonded to the surface of platen and polishing takes place by the slurry (abrasive) attached to this pad.

Examples of the abrasive cloth preferably applicable are Supreme RN available from Rodel Inc. and
5 a continuous foam suede type cloth such as Surfin IV-1 available from Fujimi Corporation. Examples of the slurry preferably applicable are colloidal-silica-based slurries with high dispersivity whose primary and secondary particle sizes of abrasive particles are not
10 more than 100 nm, such as PLANERLITE-5102 available from Fujimi Corporation or alumina-based slurries such as XJFW-8099 available from Rodel Inc., and so on.

The ultrasonic washing preferably applicable in the present invention is that for rotating an object
15 for washing (washing object) at 1000-2500 rpm and discharging pure water to which the ultrasonic wave is applied, from a swinging nozzle to the washing object to wash the washing object. The frequency of the ultrasonic wave applied is preferably not less than 800
20 kHz, taking damage of the washing object into consideration, and most preferably, it is selected from frequencies of 1 MHz to 3 MHz both inclusive.

In the present invention, the "physical washing" means general physical washing used in
25 contradistinction with the chemical washing. Specific examples of the physical washing include brush scrubbing, high-pressure jet washing, and so on. The

brush scrubbing is normally carried out as follows.

The washing object is rotated, a washing solution (pure water, a surfactant, or the like) is supplied to the washing object, and at the same time as it, a rotating

5 brush is moved on the washing object, thereby physically removing deposited particles on the washing object. Typical examples of materials for the brush are mohair, sponge, nylon, goat hair, and so on. Among these, the mohair brush and sponge brush (for example,
10 PVA (polyvinyl alcohol) sponge brush) are preferably applicable. The high-pressure jet washing method is a washing method for ejecting pure water pressurized to approximately 50 to 100 kgf/cm² by a pump, through a nozzle tip onto the surface of the washing object.
15 This washing method is also the washing carried out while rotating the washing object and swinging the jet nozzle.

A multilayer interconnection process of semiconductor device and a fabrication process of
20 reflection type liquid-crystal display device will be described as typical embodiments of the present invention. Although the following description of the processes is given by use of a semiconductor substrate, the substrate is not always limited to the
25 semiconductor substrate. For example, the substrate may be an SOI (Silicon On Insulator) substrate or a transparent substrate.

The multilayer interconnection process can be applied to fabrication processes of memory elements such as DRAM and logic elements such as MPU or ASIC.

In the following description, all switching elements of an active matrix substrate forming the liquid-crystal display device are of the MOSFET type, but they may be of the diode type, the bipolar transistor type, or the TFT type.

The reflection type liquid-crystal display device is effectively used as a display device such as a home-use television, a projector, a head-mounted display, a video conference system, or a panel of airplane.

[First Embodiment]

Fig. 1 to Fig. 7 are explanatory drawings of the multilayer interconnection fabrication process of semiconductor device according to the present invention. In Fig. 1, reference numeral 1 designates a p-type semiconductor substrate, 2 n-type wells, 3 high-concentration p⁺-type source electrodes, 4 high-concentration p⁺-type drain electrodes, and 5 gate electrodes. Low-concentration p⁻-type electric field relaxing regions 3', 4' for increasing the withstand voltage of transistor are provided around the source electrodes 3 and drain electrodes 4. Incidentally, offset amounts of the electric field relaxing regions 3', 4' are preferably 0.5 to 2.0 μm . Numeral 6 denotes selective oxide regions for element isolation.

Then, as shown in Fig. 2, NSG (non-doped glass) 7 was deposited by CVD or TEOS and thereafter this NSG 7 was polished and flattened by CMP. The CMP of NSG 7 herein was carried out preferably using an abrasive cloth, which was a lamination of a foam cloth such as IC-1000 (available from Rodel Inc.) normally used for CMP of layer insulation film and a cloth of nonwoven fabric type, and a silica-based slurry such as SC-1 (available from Cabot Inc.) using fumed silica or colloidal silica. Then p-SiN (silicon nitride film formed by the plasma CVD) 8 was deposited and subsequently, p-SiO (silicon oxide film formed by the plasma CVD) 9 was deposited. Since the p-SiN 8 is used as an etching stopper upon patterning of p-SiO 9, the thickness of the p-SiN 8 is determined to be not less than 500 Å. Since the thickness of p-SiO 9 determines the thickness of Al wiring, the thickness of p-SiO 9 needs to be equal to or greater than the thickness of necessary Al wiring for device.

Then, as shown in Fig. 3, the p-SiO 9 was patterned in wiring pattern 10 of Al by resist patterning and dry etching. Conditions of the dry etching employed herein were as follows: flow rates of etching gases $\text{CF}_4/\text{CHF}_3 = 50 \text{ ccm}/10 \text{ ccm}$; the total pressure 1000 mTorr; the power 750 W. The etch selectivity to the p-SiN 8 at this time was $\text{p-SiO etch rate}/\text{p-SiN etch rate} = 2.2$. Subsequently, the contact

pattern 11 was made by resist patterning and dry etching. Here, the interlayer film to be etched in etching of contact was the lamination of different films of p-SiN 8 and NSG 7, and thus the dry etching was two-step etching. The first-step etching conditions for etching the p-SiN 8 were $\text{CF}_4/\text{CHF}_3 = 100$ ccm/20 ccm, the total pressure 1700 mTorr, and the power 750 W; the second-step etching conditions for etching the NSG 7 and gate oxide film were $\text{CF}_4/\text{CHF}_3 = 50$ ccm/10 ccm, the total pressure 1000 mTorr, and the power 750 W.

Then wiring material 12 was deposited as shown in Fig. 4. In general, the wiring material 12 is one of metal materials such as AlSi, AlCu, or AlSiCu. When burying of contact holes 11 is conducted using the sputter reflow technology as a deposition method of those materials, the reliability of device is effectively enhanced. If a barrier metal of Ti/TiN is provided as a ground layer prior to the sputter reflow, the contact resistance will be decreased and reflow characteristics of the wiring material of AlSi or the like will be enhanced, thus facilitating the burying of contact holes 11. Another effective method for burying the contact holes 11 is a method using selective CVD of tungsten. Then the wiring material 12 was polished and flattened by metal CMP, and the wiring material was left only in the wiring pattern 10 and contact holes

11, thus forming buried wiring 13 (Fig. 5). In this case, polishing was carried out using the abrasive cloth of Surfin IV-1 available from Fujimi Corporation, the slurry of PLANERLITE-5102 available from Fujimi Corporation, and the CMP apparatus EPO-114 available from Ebara Corp. Specific polishing conditions were as follows: the load of the top ring 300 gf (gram-force)/cm²; the number of revolutions of the carrier 49 rpm; the number of revolutions of the polishing plate 50 rpm; the back side pressure 100 gf/cm²; dressing was in-situ dressing (which is dressing for simultaneously carrying out polishing and dressing) under the number of revolutions of nylon brush 51 rpm and the load thereof 42 gf/cm²; the slurry flow rate 100 ml/min.

When AlSi the Si content of which was 1 wt% was polished under the above conditions, the polishing rate 3000 Å/min and in-plane uniformity σ /polishing rate ≤ 5 % were achieved without generation of scratch in the polishing step.

Fig. 8 shows an SEM photograph of the Al surface immediately after the metal CMP. Fig. 9 is an enlarged SEM photograph of Fig. 8. It is apparent that a lot of abrasive particles 21 remain on the Al surface 20. The average density of unremovable particles 21 on the Al surface 20 was approximately 200 particles/ μm^2 . In addition to the unremovable particles 21, there remained several thousand dust particles of 0.3 μm and

more on the 6-inch wafer. Thus, such abrasive particles and dust particles have to be removed without generation of scratch by the washing step after the metal CMP.

5 When the scrubbing washing with the PVA brush often used in general was applied to the washing of the Al surface after the metal CMP, there appeared many scratches 22 shown in the optical microscope photograph of Fig. 10. Relatively large particles or aggregate
10 particles that existed on the Al surface before the washing are considered to be the cause of the scratches. It is thus necessary to wash the dust particles or abrasive particles, which could be the cause of scratch, away by a physical non-contact
15 technique before the brush scrubbing washing for physically scraping the surface.

 The inventor used the megasonic washing for washing the surface of wafer with a flow of pure water loaded with high-frequency vibration. Conditions of
20 megasonic pure water were determined so that the vibration of the frequency 1.5 MHz and the power 48 W was applied from an oscillator provided in a nozzle to the pure water flowing at the rate of 1 l/min through the tip of the nozzle having the diameter 6 mm ϕ . It
25 was verified that the washing effect of abrasive particles on the Al surface by the megasonic washing depended upon the number of revolutions of the wafer

upon washing as shown in Fig. 11. Each of 0 mm, 30 mm, and 60 mm described in Fig. 11 indicates a distance from the center of wafer to a measurement point and conditions of the megasonic nozzle are the scan speed: 10 mm/sec and the number of scans: 20. As seen from Fig. 11, the number of revolutions of wafer upon the megasonic washing is preferably not less than 1500 rpm and more preferably not less than 2000 rpm. Fig. 33 is an explanatory drawing to show the configuration of a washing device. As shown in Fig. 33, the nozzle 51 for discharging the washing solution is movable above the wafer 52. Arrows 53 indicate moving directions of the nozzle.

Next examined was washing water vibration frequency dependence of the washing effect of abrasive particles on the Al surface. The results are shown in Fig. 15. In this examination, measurements were conducted under such conditions that the number of revolutions of wafer upon washing was 2000 rpm, the scan speed of the washing water nozzle was 10 mm/sec, the number of scans of the nozzle was 20, and frequencies were varied. It is understood from the drawing that the removing effect of particles adhering to the Al surface starts appearing when the frequency of vibration loaded on the washing water becomes 800 kHz and that the extremely great washing effect appears in the region of frequencies of the MHz order.

In general, the washing using low frequencies ranging from several ten kHz to approximately 400 kHz is a washing method for removing the dust particles of sizes from several μm to several ten μm on the surface of substrate by applying strong shock waves to the surface of substrate through liquid cavitation resulting from liquid resonance. This washing method has the problem that the shock by this liquid cavitation could damage micropatterns. Therefore, it is not used in semiconductor processes of 4M-DRAM and after. In the examination by the inventor, the problem of exfoliation of patterned Al arose in the washing at 80 kHz and 400 kHz. On the other hand, no damage of pattern was recognized at high frequencies of not less than 800 kHz.

Taking the above washing effect and pattern damage into consideration, use of high frequencies of not less than 800 kHz is effective for washing of abrasive particles adhering to the Al surface. It is understood that the frequency is determined more preferably in the range of 1 MHz to 3 MHz both inclusive.

Next, the Al surface was washed under such conditions that the frequency was 1.5 MHz, the number of revolutions of the wafer was 2000 rpm, the scan speed of the nozzle was 10 mm/sec, and the number of scans of the nozzle was 20. As a result, the particles on the Al surface were removed down to the density of

30 particles/ μm^2 or less. Fig. 12 shows an SEM photograph of the Al surface washed under the above conditions. The distance from the center of wafer to the measurement point in Fig. 12 is 30 mm. In the photograph numeral 20' denotes the Al surface and 21' abrasive particles. The dust particles of 0.3 μm and greater were able to be removed to approximately several ten particles on the 6-inch wafer. Fig. 13 shows the results of measurement of particles of 0.3 μm and greater by particle examining apparatus IS-3270 available from Hitachi, Ltd. During the above megasonic washing the back face of wafer was always kept in a wet state with shower of pure water.

Then simultaneous brush scrubbing washing was conducted to clean the Al surface after the megasonic washing with a pencil type PVA sponge and to clean the back face of wafer with a roll type PVA sponge. The washing conditions were as follows. For the Al surface, a pressing amount of the pencil type PVA sponge was 1 mm, the number of revolutions of the sponge was 60 rpm, the number of revolutions of the wafer was 100 rpm, the scan speed of the pencil type PVA sponge was 10 mm/sec, and the number of scans was 3. For the back face of wafer, a pressing amount of the roll type PVA sponge was 1 mm, the number of revolutions of the roll sponge was 100 rpm, and the washing time was 60 seconds. Further, the megasonic

washing was again carried out after the scrubbing washing. The washing conditions were exactly the same as the aforementioned megasonic washing conditions except that the number of scans of the nozzle was 3.

5 After that, the wafer was dried by spin drying at the number of revolutions of wafer of 2300 rpm for 30 seconds. Fig. 14 shows an SEM photograph of the Al surface having resulted after the above washing operations. In the photograph numeral 20" indicates
10 the Al surface. It is seen that the abrasive particles and dust particles are removed clean.

Next, as shown in Fig. 6, a lamination of second layer p-SiN 8' and second layer p-SiO 9' were successively deposited and thereafter second layer
15 buried wiring 13' was formed by the same method as the dual damascene as described referring to Fig. 3 to Fig. 5. Then buried wiring 13" of third layer was formed by the same technique, as shown in Fig. 7. In the drawing numeral 8" denotes third layer p-SiN and 9" third layer
20 p-SiO. It is needless to mention that buried wiring of the fourth layer and after can be further formed by the like dual damascene. The material for the buried wiring of each layer can also be selected from highly
25 electroconductive materials such as Ag, Au, Pt, Cr, or Cu.

In the present embodiment the wafer surface with exposed metal after formation of the buried wiring was

subjected to the following washing after the metal CMP
of the dual damascene process. After completion of the
polishing, the surface was first subjected to the
ultrasonic washing, then to the scrubbing washing with
5 the PVA sponge or mohair brush, and further to the
megasonic (ultrasonic) washing. Thereafter, the wafer
was dried by spin drying. It is, however, noted that
the point of the present invention is to carry out the
ultrasonic washing prior to the physical washing and
10 that the present invention is by no means limited to
the embodiment described herein.

The washing effect of the above scrubbing washing
is further enhanced by carrying out a plurality of
washing processes in a plurality of different washing
15 units. By employing the above washing sequence, the
washing with extremely high cleanliness is achieved
without generation of scratch in the surface of wiring
material and over the entire surface of wafer, so that
highly reliable semiconductor devices can be provided
20 at high yield.

[Second Embodiment]

An example of application wherein the present
invention is applied to a fabrication process of the
active matrix substrate of reflection type liquid-
25 crystal display device will be described referring to
Fig. 16 to Fig. 25.

In Fig. 16, numeral 1 designates a p-type

semiconductor substrate, 2 n-type wells, 3 high-concentration p⁺-type source electrodes, 4 high-concentration p⁺-type drain electrodes, and 5 gate electrodes. Low-concentration p⁻-type electric field relaxing regions 3', 4' for increasing the withstand voltage of transistor are provided around the source electrodes 3 and drain electrodes 4. Incidentally, offset amounts of the electric field relaxing regions 3', 4' are preferably 0.5 to 2.0 μm . Numeral 6 denotes selective oxide regions for element isolation.

Then, as shown in Fig. 17, NSG (non-doped glass) 7 was deposited by CVD or TEOS and thereafter this NSG 7 was polished and flattened by CMP. The CMP of NSG 7 herein was carried out preferably using the abrasive cloth, which was the lamination of the foam cloth such as IC-1000 normally used for CMP of layer insulation film and the cloth of nonwoven fabric type, and the silica-based slurry such as SC-1 using fumed silica or colloidal silica. Then p-SiN (silicon nitride film formed by the plasma CVD) 8 was deposited and subsequently, p-SiO (silicon oxide film formed by the plasma CVD) 9 was deposited. Since the p-SiN 8 is used as an etching stopper upon patterning of p-SiO 9, the thickness of the p-SiN 8 is not less than 500 Å. Since the thickness of p-SiO 9 determines the thickness of Al wiring, the thickness of p-SiO 9 needs to be equal to or greater than the thickness of necessary Al wiring

for device.

Then, as shown in Fig. 18, the p-SiO 9 was patterned in wiring pattern 10 of Al by resist patterning and dry etching. Conditions of the dry etching employed herein were as follows: flow rates of etching gases $\text{CF}_4/\text{CHF}_3 = 50 \text{ ccm}/10 \text{ ccm}$; the total pressure 1000 mTorr; the power 750 W. The etch selectivity to the p-SiN 8 at this time was p-SiO etch rate/p-SiN etch rate = 2.2. Subsequently, the contact pattern 11 was made by resist patterning and dry etching. Here, the interlayer film to be etched in etching of contact was the lamination of different films of p-SiN 8 and NSG 7, and thus the dry etching was two-step etching. The first-step etching conditions for etching the p-SiN 8 were $\text{CF}_4/\text{CHF}_3 = 100 \text{ ccm}/20 \text{ ccm}$, the total pressure 1700 mTorr, and the power 750 W; the second-step etching conditions for etching the NSG 7 and gate oxide film were $\text{CF}_4/\text{CHF}_3 = 50 \text{ ccm}/10 \text{ ccm}$, the total pressure 1000 mTorr, and the power 750 W.

Then wiring material 12 was deposited as shown in Fig. 19.

Then the wiring material 12 was polished and flattened by the metal CMP, and the wiring material was left only in the wiring pattern 10 and contact holes 11, thus forming buried wiring 13 (Fig. 20). The method for forming the buried wiring 13 described above

is the same as in the first embodiment.

After completion of the polishing by CMP, p-SiO 30 was deposited and then shield layer 31 was deposited as shown in Fig. 21. Materials effectively applicable for the shield layer 31 are metal materials such as Ti, Mo, Al, W, Ag, Pt, or Cr, and in this embodiment Ti was deposited in the thickness of 2000 Å. The shield layer 31 was then patterned.

Then, as shown in Fig. 22, p-SiO 33 was deposited in the thickness of 1000 Å or more, and the p-SiO 33 was patterned using the shield layer 31 as an etching stopper. Subsequently, capacitance film 34 was deposited. Materials effectively applicable for the capacitance film 34 are highly dielectric materials such as p-SiN or Ta₂O₅, and in this embodiment p-SiN was deposited in the thickness of 4000 Å.

Next, as shown in Fig. 23, the capacitance film 34 and p-SiO 30 were patterned and then reflective electrode material 35 was deposited in the thickness greater than that of p-SiO 33. Materials suitable for the reflective electrode are electroconductive materials with high reflectivity in visible light region, such as Al, Ag, Pt, or Cr. In the present embodiment Al was used.

Then, as shown in Fig. 24, the reflective electrode material 35 was polished and flattened by the CMP. A polishing amount was so determined that the

surface was polished so as to expose p-SiO 33 in the wafer surface. In this embodiment the reflective electrode 36 was formed by the metal CMP of Al. The conditions upon the aforementioned formation of buried wiring 13 also apply correspondingly to the conditions of the metal CMP of Al and the washing after the polishing.

Then reflection enhancing film 37 was deposited as shown in Fig. 25. A material for the reflection enhancing film 37 is selected from dielectrics with high refractive index such as ZnS or TiO_2 , and the reflection enhancing film 37 is deposited in the thickness equal to a quarter of the wavelength of light used in the display device. A more effective structure is a lamination of layers with increasing refractive indices from the bottom and each in the thickness equal to a quarter of the above wavelength of light, such as p-SiO/p-SiN/ TiO_2 .

The feature of the present embodiment is that in the washing after the metal CMP for formation of the reflective electrode 36 by dual damascene, the wafer surface is first washed by megasonic washing after completion of polishing and subsequently it is washed by physical washing. By employing such washing sequence, the reflective electrode 36 with clean surface is realized without any scratch, and a high-luminance and high-definition reflection type liquid-crystal display device can be provided.

WHAT IS CLAIMED IS:

1. A fabrication method of semiconductor device comprising a step of forming an electroconductive material film on a substrate, a step of polishing the electroconductive material film, and a step of washing a polished surface of said electroconductive material film,

wherein said washing step is a step of carrying out ultrasonic washing with a washing solution to which an ultrasonic wave is applied, prior to physical washing.

2. A fabrication method of semiconductor device according to Claim 1, wherein said polishing step is carried out by use of CMP (Chemical Mechanical Polishing).

3. A fabrication method of semiconductor device according to Claim 1, wherein said ultrasonic washing is carried out in a frequency band of not less than 800 kHz.

4. A fabrication method of semiconductor device according to Claim 3, wherein said frequency band is a range of 1 MHz to 3 MHz both inclusive.

5. A fabrication method of semiconductor device

according to Claim 1, wherein said ultrasonic washing is carried out while said washing solution is discharged from a nozzle.

5 6. A fabrication method of semiconductor device according to Claim 1, wherein said ultrasonic washing is carried out while the substrate with said polished surface thereon is rotated at 1000-2500 rpm.

10 7. A fabrication method of semiconductor device according to Claim 1, wherein said physical washing is selected from brush scrubbing and high-pressure jet washing.

15 8. A fabrication method of semiconductor device according to Claim 7, wherein said brush scrubbing is carried out using either a mohair brush or a sponge brush.

20 9. A fabrication method of semiconductor device according to Claim 8, wherein PVA (polyvinyl alcohol) is used for said sponge.

25 10. A fabrication method of semiconductor device according to Claim 1, wherein ultrasonic washing is again carried out after said physical washing.

A fabrication method of semiconductor device comprising a step of forming an electroconductive material film on a substrate, a step of polishing the electroconductive material film, and a step of washing a polished surface of the electroconductive material film, wherein the washing step is a step of carrying out ultrasonic washing with a washing solution to which an ultrasonic wave is applied, prior to physical washing.

10

FIG. 1

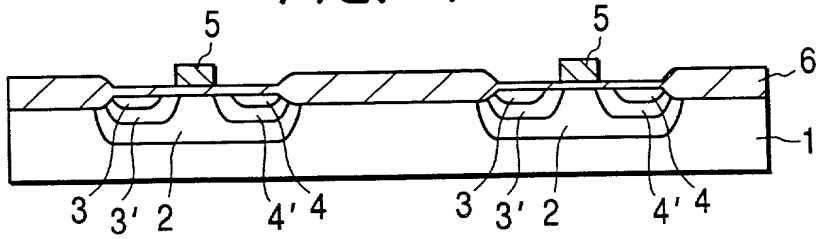


FIG. 2

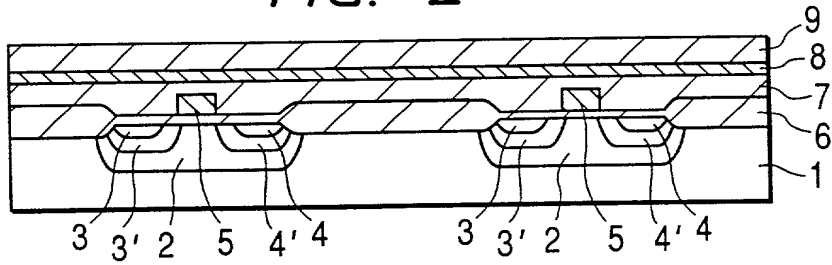


FIG. 3

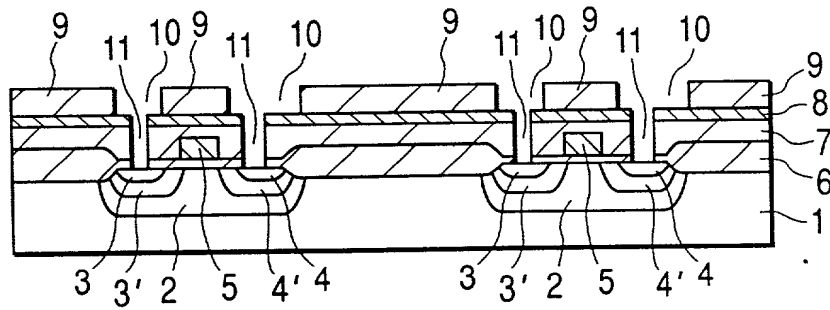


FIG. 4

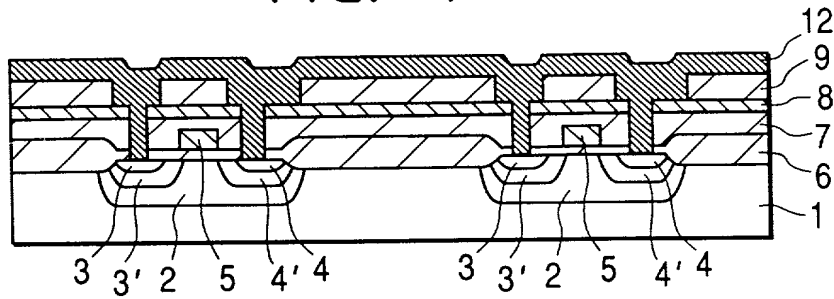


FIG. 5

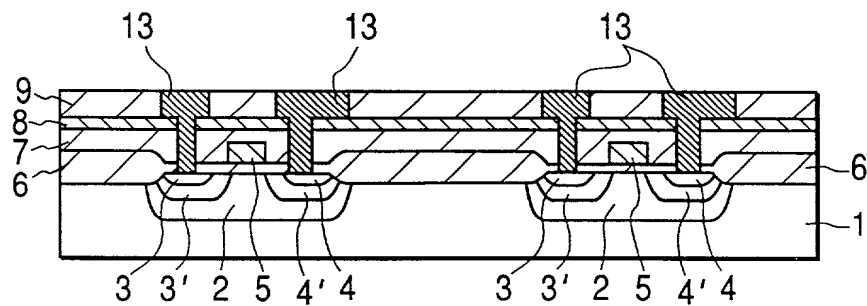


FIG. 6

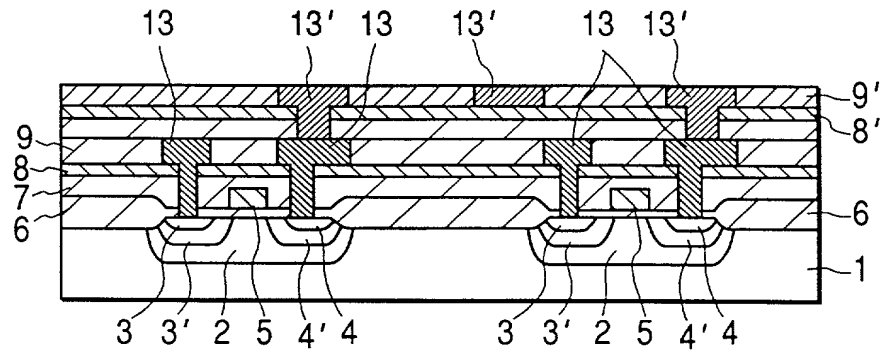


FIG. 7

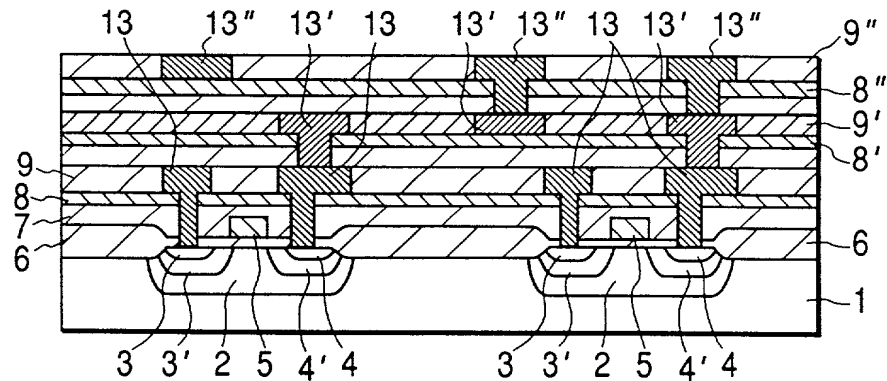


FIG. 8

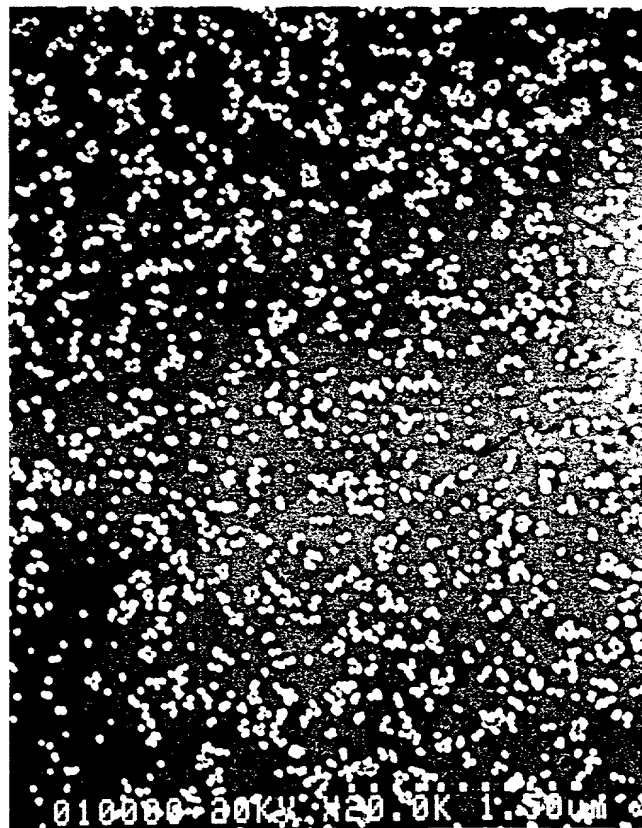


FIG. 9

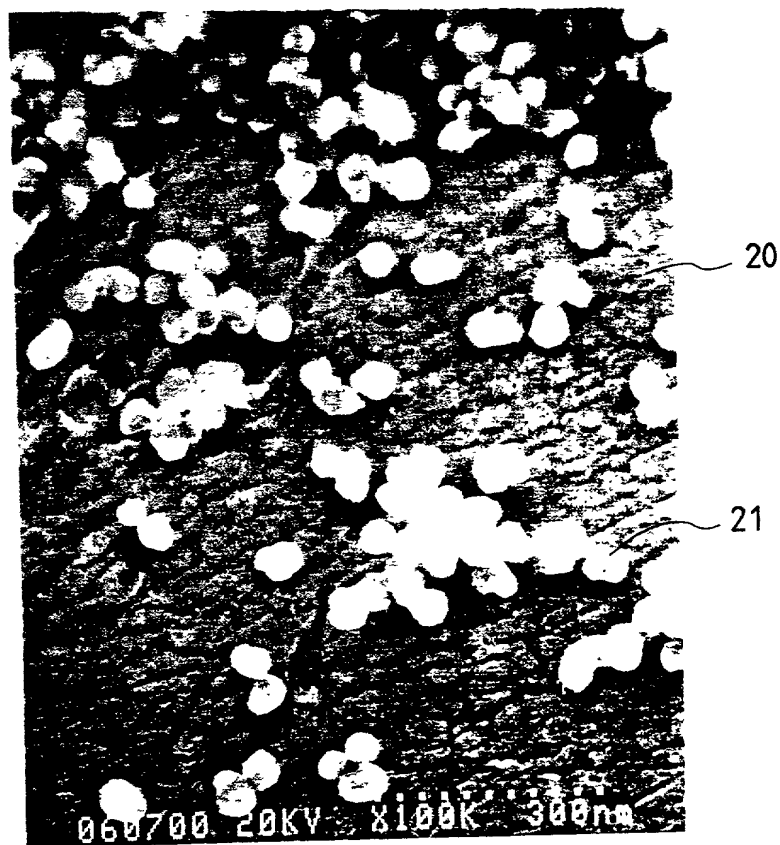


FIG. 10

22

DATE: 96/07/30 18:22

LENS NO. :5

LEVEL: 0.23:L1 X= 96120 Y= 67384

FIG. 11

□	500rpm	0mm
●	500rpm	30mm
△	500rpm	60mm
□	1500rpm	0mm
●	1500rpm	30mm
△	1500rpm	60mm
□	2000rpm	0mm
●	2000rpm	30mm
△	2000rpm	60mm
■	NO WASHING	

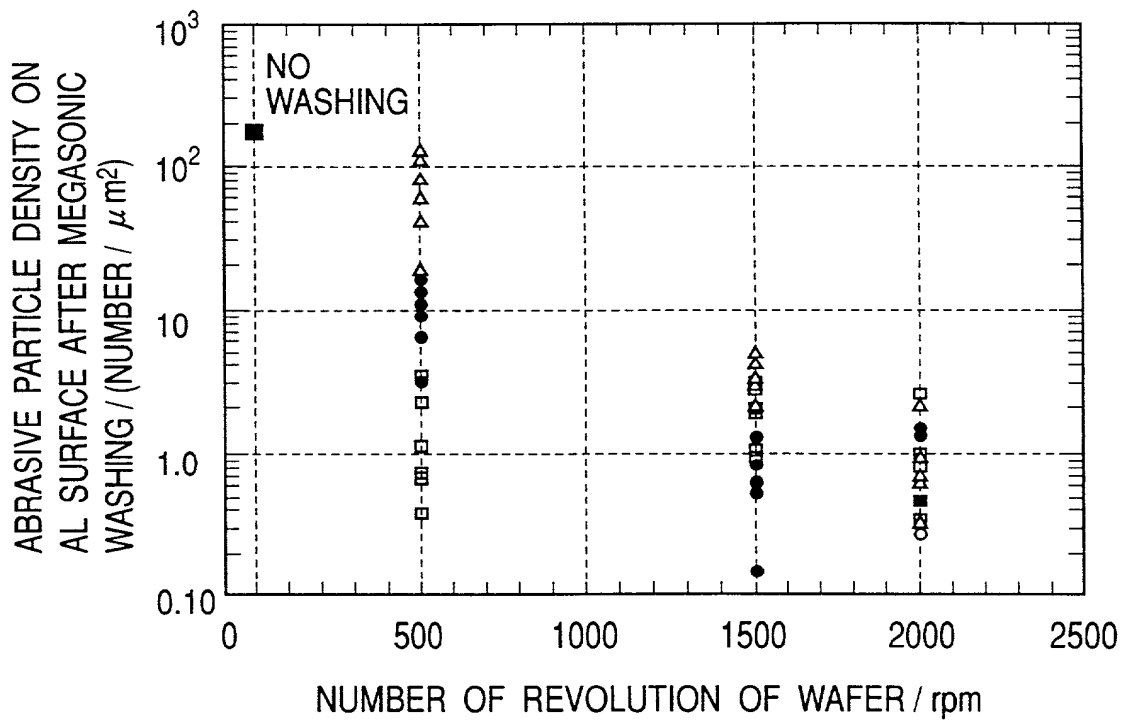
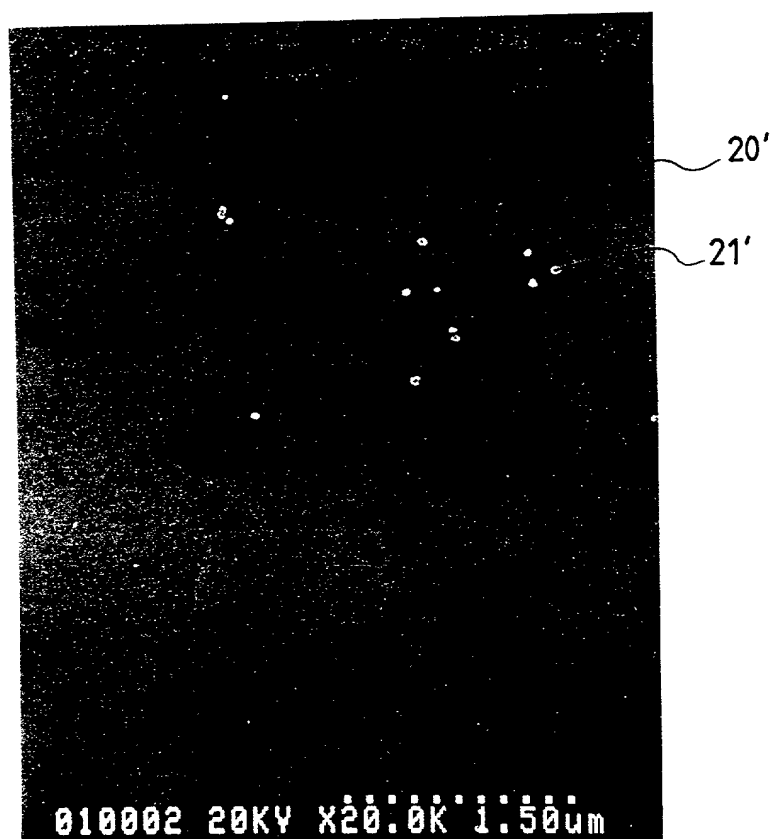


FIG. 12



2000rpm, 30mm

FIG. 13

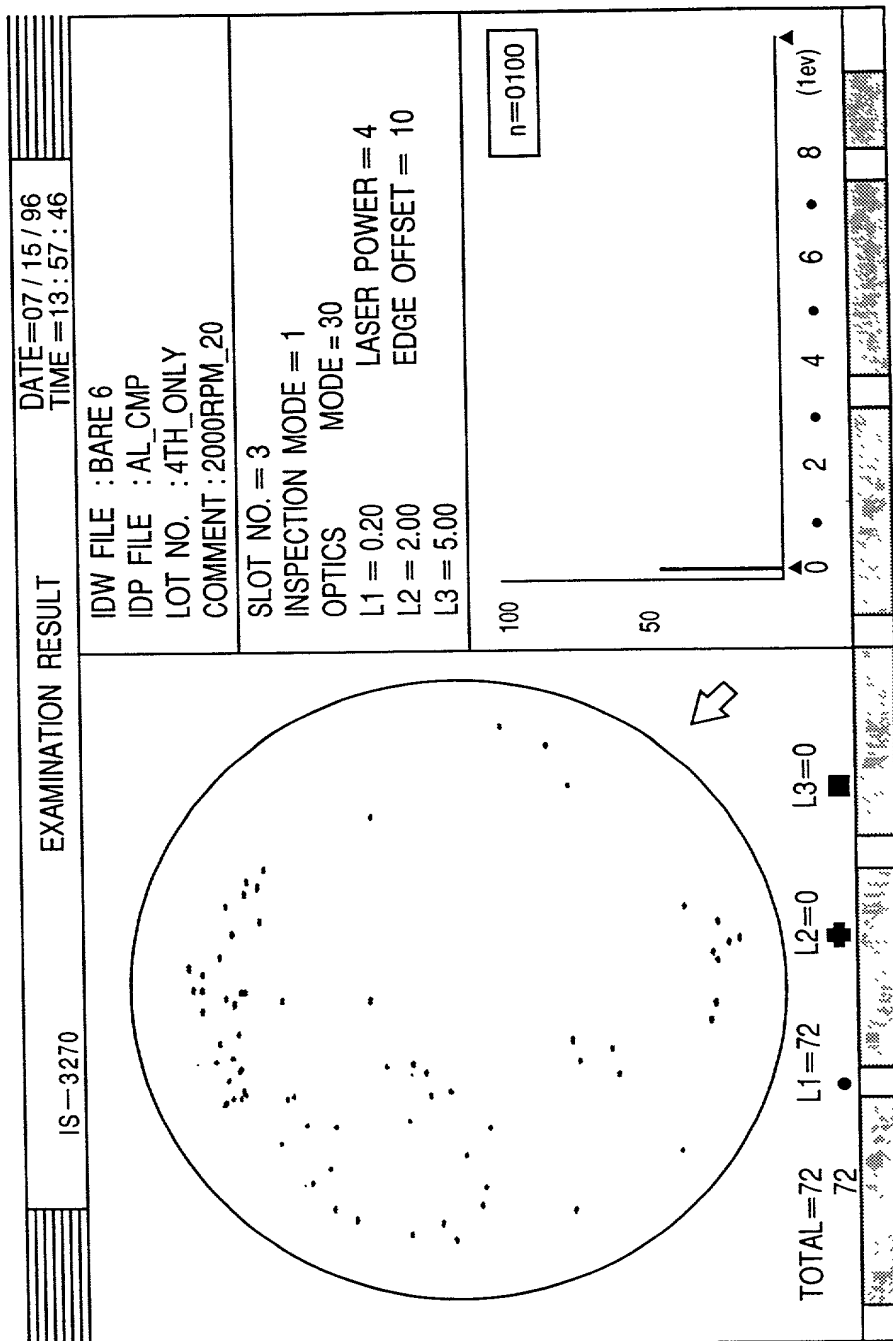


FIG. 14

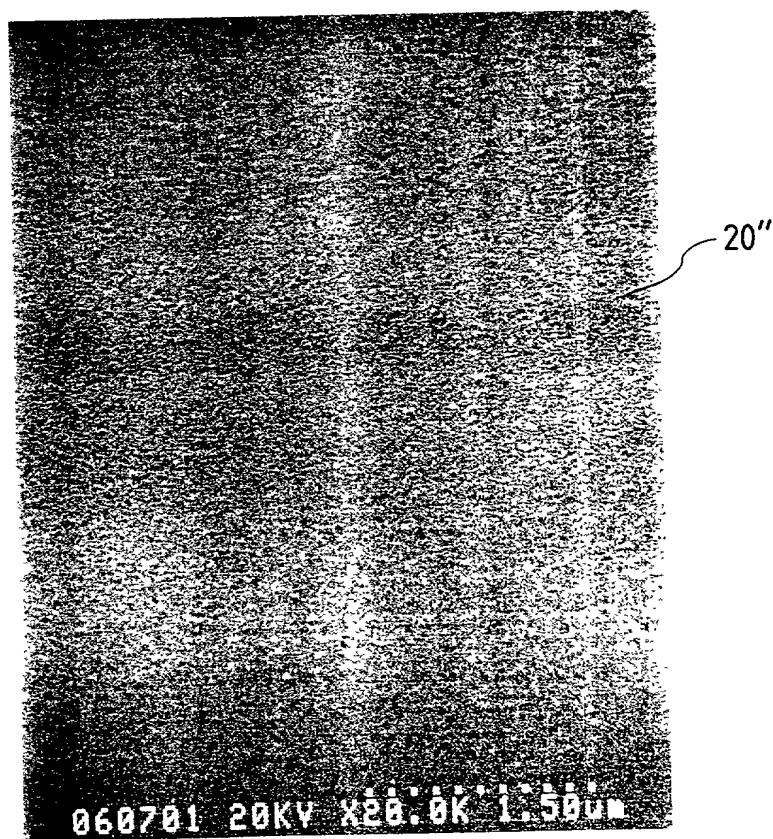


FIG. 15

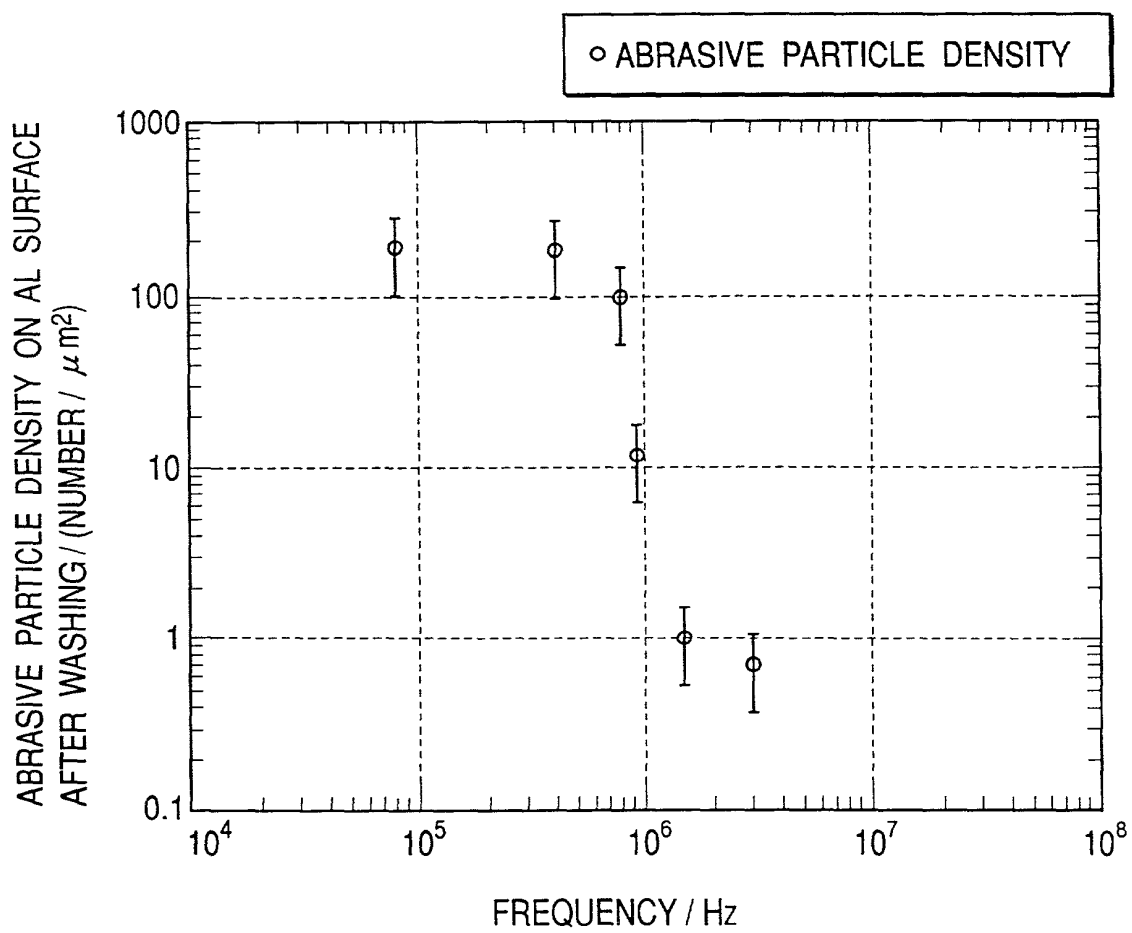


FIG. 16

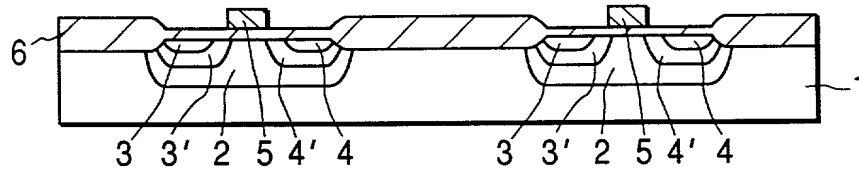


FIG. 17

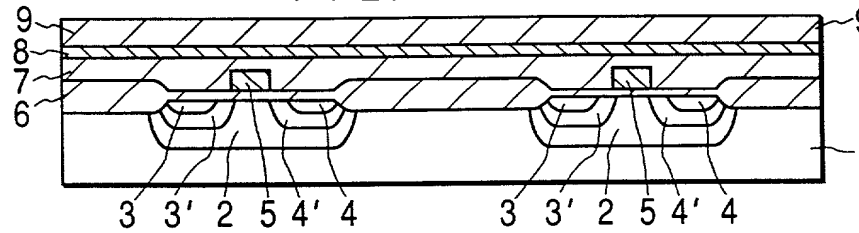


FIG. 18

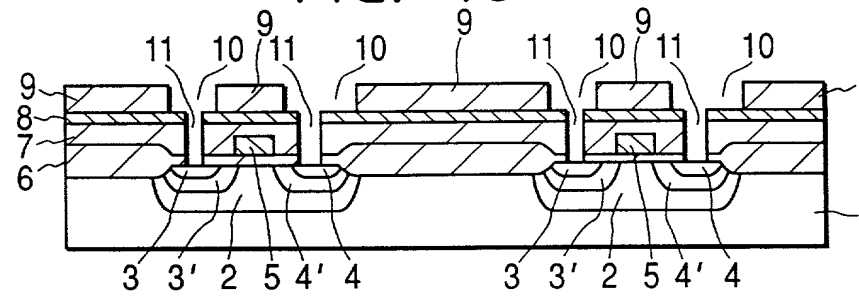


FIG. 19

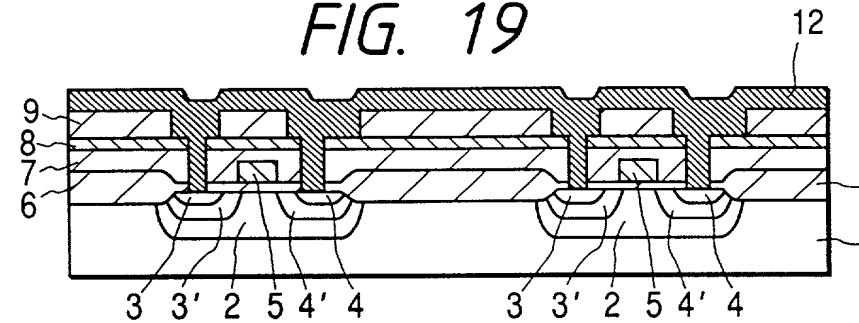


FIG. 20

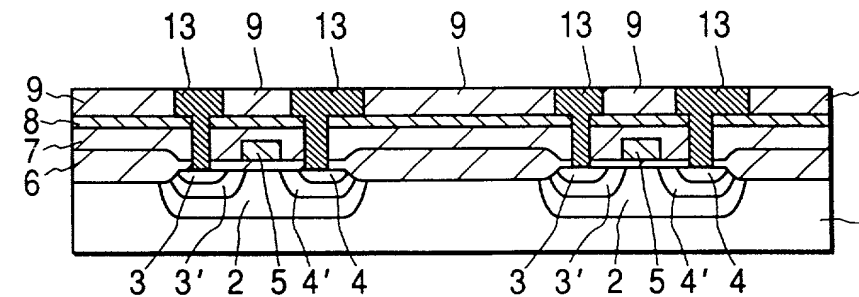


FIG. 21

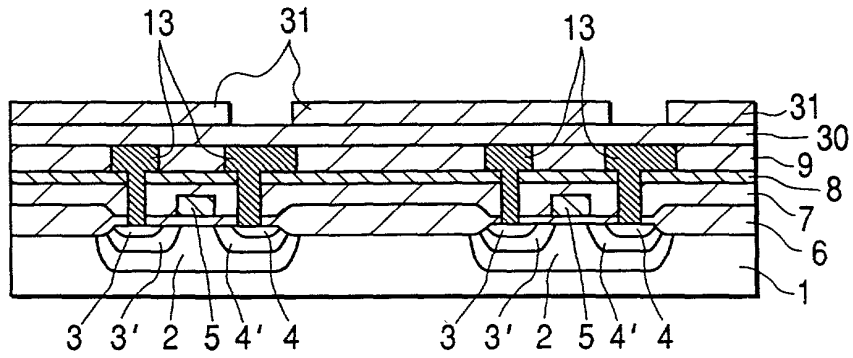


FIG. 22

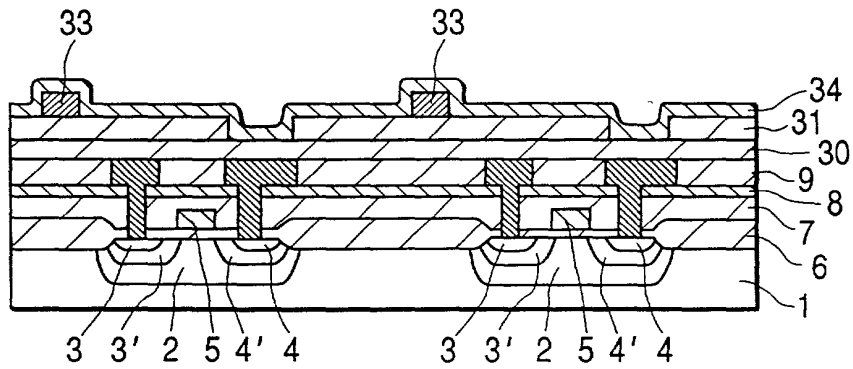


FIG. 23

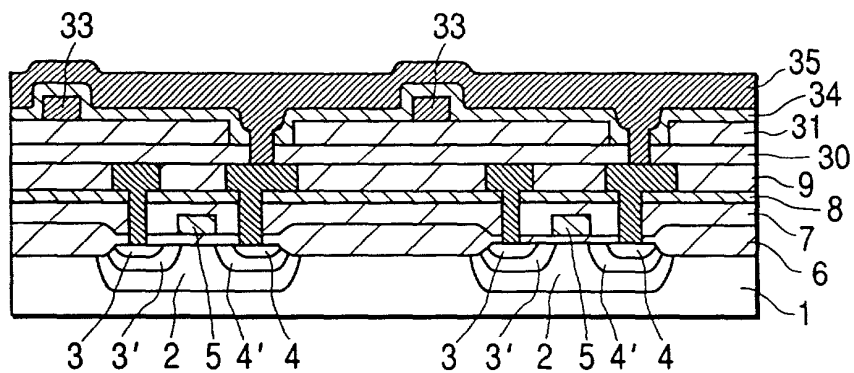


FIG. 24

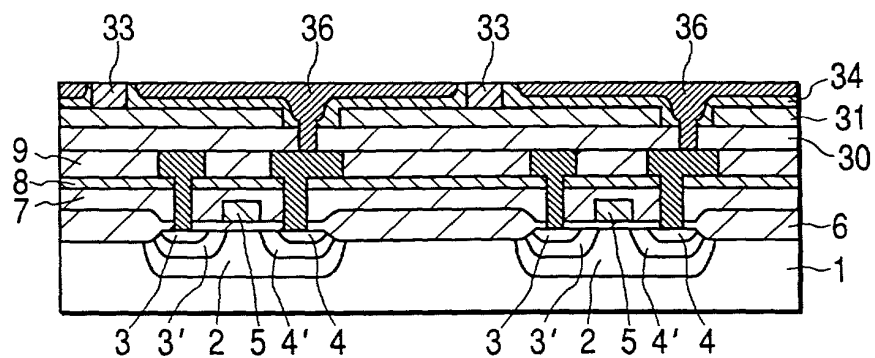


FIG. 25

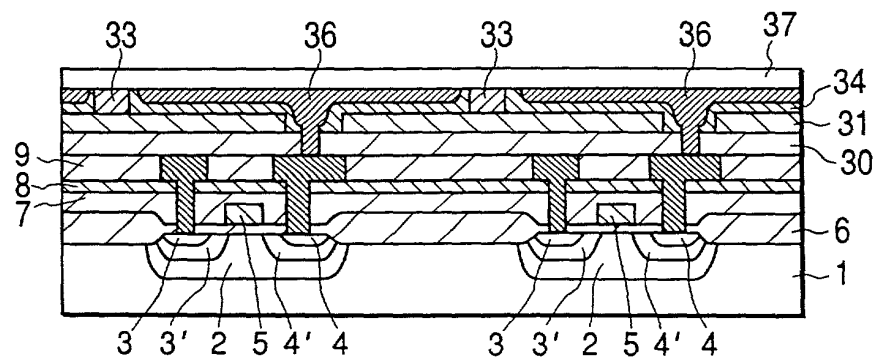


FIG. 26

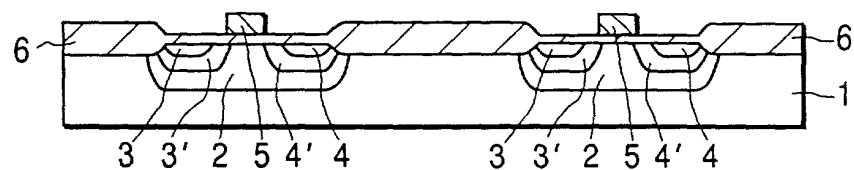


FIG. 27

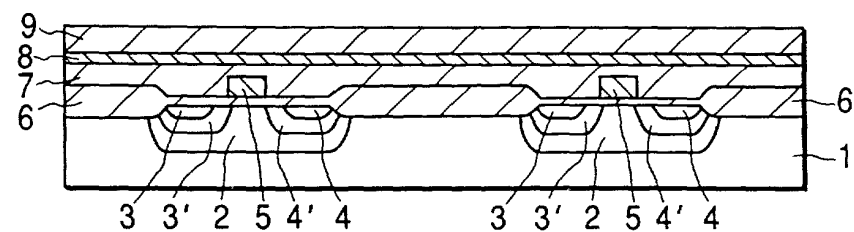


FIG. 28

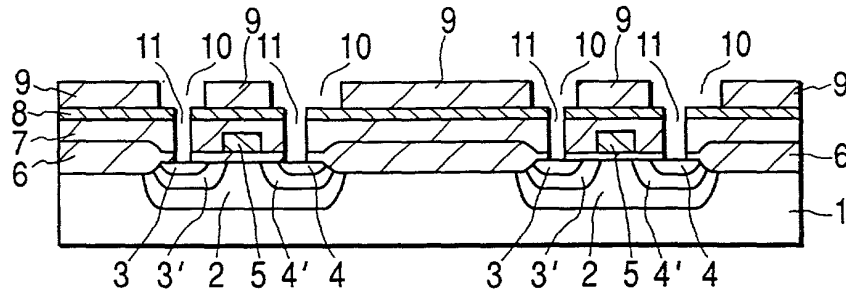


FIG. 29

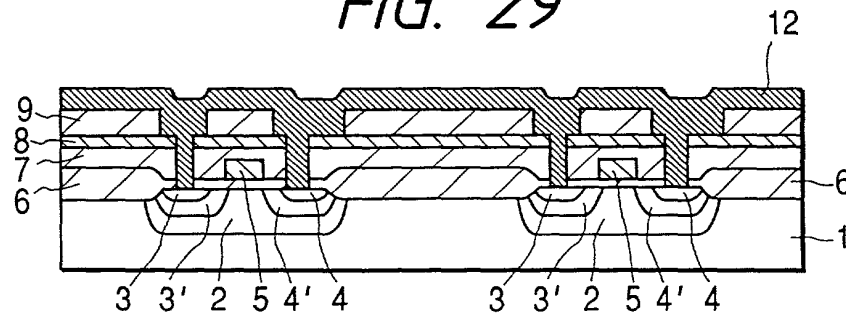


FIG. 30

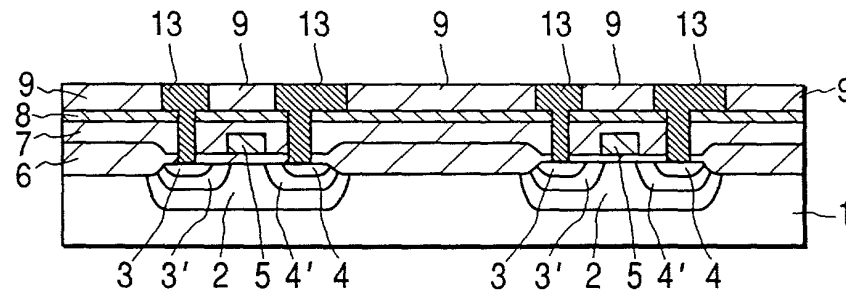


FIG. 31

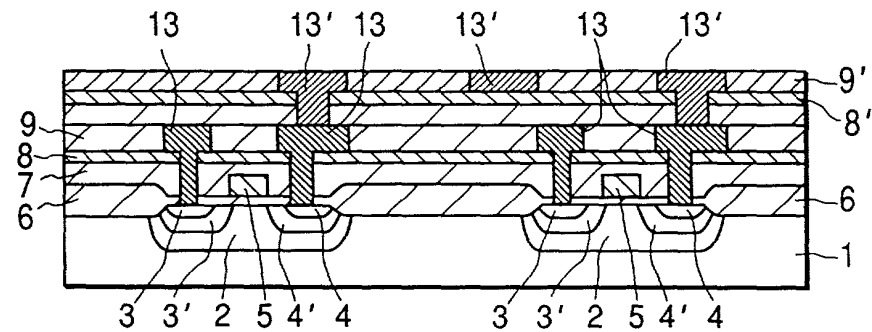


FIG. 32

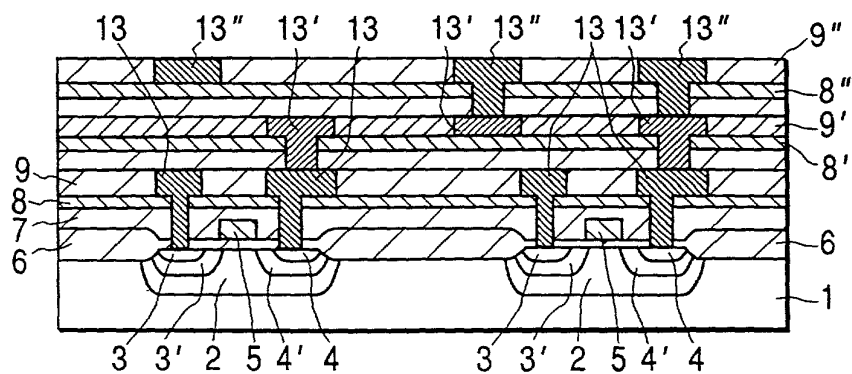
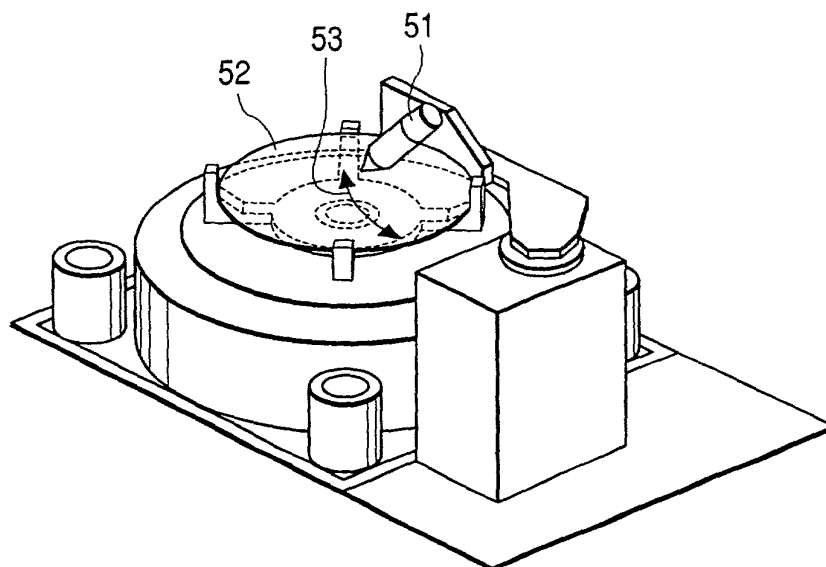


FIG. 33



**COMBINED DECLARATION AND POWER OF ATTORNEY
FOR C-I-P PATENT APPLICATION**

As a below named inventor, I hereby declare that.

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
_____, the specification of which

☒ attached hereto. ☐ was filed on _____
as Application No. _____ and was amended on _____
(if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Country	Application No.	Filed (Day/Mo./Yr.)	(Yes/No) Priority Claimed
Japan	07-236865	14 September 1995	Yes
Japan	08-241939	12 September 1996	Yes
Japan	08-319568	26 November 1996	Yes

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Filed (Day/Mo./Yr.)	Status (Patented/Pending/Abandoned)
08/714,437	16 September 1996	Pending
08/979,957	26 November 1997	Pending

I hereby appoint the practitioners associated with the firm and Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to the address associated with that Customer Number:

FITZPATRICK, CELLA, HARPER & SCINTO
Customer Number: 05514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

COMBINED DECLARATION AND POWER OF ATTORNEY
FOR C-I-P PATENT APPLICATION

(Page 2)

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Second Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____

Post Office Address _____

Full Name of Third Joint Inventor, if any _____

Third Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____

Post Office Address _____

Full Name of Fourth Joint Inventor, if any _____

Fourth Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____

Post Office Address _____

Full Name of Fifth Joint Inventor, if any _____

Fifth Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____

Post Office Address _____

Full Name of Sixth Joint Inventor, if any _____

Sixth Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____

Post Office Address _____